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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,857	03/15/2004	Mitsuaki Osame	12732-219001	2041

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FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
HO, BINH VAN	
ART UNIT	**PAPER NUMBER**
2821	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,857	OSAME ET AL.	
	Examiner	Art Unit	
	Binh V. Ho	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2 to 5, 7 to 10, 11 to 15, 17 to 20, 22 to 25, 27 to 30, 32 to 35 and 37 to 40 are objected to because of the following informalities:

In claims 2 to 5, 7 to 10, 11 to 15, 17 to 20, 22 to 25 and 27 to 30, lines 1, "A device" should be changed to --The device--.

In claims 32 to 35 and 37 to 40, lines 1, "A substrate" should be changed to --The substrate --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 6, 11, 16, 21, 26, 31 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Koyama (6,753,654).

(Claim 1)

Koyama teaches in figure 2, a light emitting device (101) comprising a light emitting element (104) provided in a pixel, a first transistor (Tr2) provided in pixel for

determining a current value flowing in the light emitting element (104), and a second transistor (Tr1) provided in pixel for determining a light emission or non-emission of the light emitting element (104) according to a video signal (Si), wherein the light emitting element (104) is connected in series to the first transistor (Tr2) and the second transistor (Tr1) between a first power supply (Vi) and a second power supply (Vx), a gate electrode of the first transistor (Tr2) is connected to the first power supply (Vi), and the first transistor (Tr2) is a depletion mode transistor.

(Claim 6)

Koyama teaches a light emitting device (101) comprising a light emitting element (104) provided in a pixel; a first transistor (Tr2) provided in said pixel for determining a current value flowing in the light emitting element(104), and a second transistor (Tr1) provided in said pixel for determining a light emission or non-emission of the light emitting element (104) according to a video signal (Si), wherein the light emitting element (104) is connected in series to the first transistor (Tr2) and the second transistor (Tr1) between a first power supply (Vi) and a second power supply (Vx), a gate electrode of the first transistor (Tr2) is connected to either a source electrode or a drain electrode of the first transistor (Tr2), and the first transistor (Tr2) is a depletion mode

(Claim 11)

Koyama teaches a light emitting device (101) comprising a light emitting element (104) provided in a pixel; a first transistor (Tr2) provided in said pixel for determining a current value flowing in the light emitting element (104); and a second transistor (Tr1)

provided in said pixel for determining a light emission or non-emission of the light emitting element (104) according to a video signal(Si), and a third transistor (Tr4) provided in said pixel for controlling input of said video signal (Vi), wherein the light emitting element (104) is connected in series to the first transistor (Tr2) and the second Transistor (Tr1) between a first power supply (Vi) and a second power supply (Vx) a gate electrode of the first transistor (Tr2) is connected to the first power supply (Vi) and the first transistor (Tr2) is a depletion mode transistor.

(Claim 16)

Koyama teaches a light emitting device (101) comprising a light emitting element (101) provided in a pixel, a first transistor (Tr2) provided in said pixel for determining a current value flowing in the light emitting element (104) a second transistor (Tr1) provided in said pixel for determining a light emission or non-emission of the light emitting element (104) according to a video signal(Si) and a third transistor (Tr4) provided in said pixel for controlling input of said video signal (Si), wherein the light emitting element (104) is connected in series to the first transistor (Tr2) and the second transistor (Tr1) between a first power supply (Vi) and a second power supply (Vx), a gate electrode of the first transistor (Tr2) is connected to either a source electrode or a drain electrode of the first transistor (Tr2) and the first transistor (Tr2) is a depletion mode transistor.

(Claim 21)

Koyama teaches a light emitting device (101) comprising a light emitting element (104) provided in a pixel, a first transistor (Tr2) provided in said pixel for determining a

current value flowing in the light emitting element (104) a second transistor (Tr1) provided in said pixel for determining a light emission or non-emission of the light emitting element (104) according to a video signal (Si) a third transistor (Tr4) provided in said pixel for controlling an input of the video signal (Vi) and a fourth transistor (Tr3) provided in said pixel for setting the light emitting element (104) in a non-emission state regardless of the video signal (Si), wherein the light emitting element (104) is connected in series to the first transistor (Tr2)and the second transistor (Tr1) between a first power supply (Vi) and a second power supply (Vx) a gate electrode of the first transistor (Tr2) is connected to the first power supply (Vi) and the first transistor (Tr2) is a depletion mode transistor.

(Claim 26)

Koyama teaches a light emitting device (101) comprising a pixel comprising a light emitting element (104) provided in a pixel, a first transistor (Tr2) provided in said pixel for determining a current value flowing in the light emitting element (104), a second transistor (Tr1) provided in said pixel for determining a light emission or non-emission of the light emitting element (104) according to a video signal (Si) a third transistor (Tr4) provided in said pixel for controlling an input of the video Signal (Si) and a fourth transistor (Tr3) provided in said pixel for setting the light emitting element (104) in a non-emission state regardless of the video signal (Si), wherein the light emitting element (104) is connected in series to the first transistor (Tr2) and the second transistor (Tr1) between a first power supply (Vi) and a second power supply (Vx) a gate electrode of the first transistor (Tr2) is connected to either a source electrode or a

drain electrode of the first transistor (Tr2), and the first transistor (Tr2) is a depletion mode transistor.

(Claim 31)

Koyama teaches a first transistor (Tr2) provided in said pixel (101) for determining a current value flowing in the pixel electrode (104), and a second transistor (Tr1) provided in said pixel (101) for determining a current supply or no current supply to the pixel electrode (104) according to a video signal (Si), wherein the first transistor (Tr2) is connected in series to the second transistor (Tr1) between a first power supply (Vi) and the pixel electrode (104), a gate electrode of the first transistor (Tr2) is connected to the first power supply (Vi) and the first transistor (Tr2) is a depletion mode transistor.

(Claim 36)

Koyama teaches a first transistor (Tr2) provided in said pixel for determining a current value flowing in the pixel electrode (104) and a second transistor (Tr1) provided in said pixel for determining a current supply or no current supply to the pixel electrode (104) according to a video signal (Si), wherein the first transistor (Tr2) is connected in series to the second transistor (Tr1) between a first power supply (Vi) and the pixel electrode (104) a gate electrode of the first transistor (Tr2) is connected to either a source electrode or a drain electrode of the first transistor (Tr2) and the first transistor (Tr2) is a depletion mode transistor.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 11 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishitoba (US20020196212).

Nishitoba teaches in figure 3, a light emitting device comprising a light emitting element (11) provided in a pixel, a first transistor (8) provided in pixel for determining a current value flowing in the light emitting element (11), a second transistor (9) an a third transistor (12) provided in pixel for determining a light emission or non-emission of the light emitting element (11) according to a video signal (3), wherein the light emitting element (11) is connected in series to the first transistor (8) and the second transistor (9) between a first power supply (1) and a second power supply, a gate electrode of the first transistor (8) is connected to the first power supply (3), and the first transistor (8) is a depletion mode transistor.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 7-10, 12-15, 17-20, 22-25, 27-30, 32-35 and 37-40 are rejected under 35 U.S.C. 103(a) as being anticipated by (6,753,654).

Koyama teaches all of the elements, including each of the first transistor and the second transistor has a P-type and N-type (col. 6, lines 27-28). Koyama, does not disclose a threshold potential of the first transistor is higher or lower than a threshold potential of the second transistor; the channel length of the first transistor is longer than its channel width, and a channel length of the second transistor is equal to or shorter than its channel width; and the ratio of the channel length to the channel width of the first transistor is five or more. However, it would have been obvious to one having ordinary skill in the art, at the time the invention, to select the transistor with the specific threshold potential, channel length, channel width and ratio of channel length versus channel width. Since it has been hold to be within the general skill in the art to choose the value of transistor's parameter in order to achieve particularly desired results involves only routine in the art (refer to the document title "MOS Transistor Terminals" attached).

Inquiry

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh V. Ho whose telephone number is 571 272 8583. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don K. Wong can be reached on 571 272 1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Primary

BinhV Ho
Examiner
Art Unit 2821

BinhVan Ho
07/05/2005